# *Q-enhancement with on-chip inductor optimization for reconfigurable Δ-Σ radio-frequency ADC*


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***Abstract*—The paper details on-chip inductor optimization for a reconfigurable continuous-time delta-sigma (Δ-Σ) modulator based radio-frequency analog-to-digital converter. Inductor optimisation enables the Δ-Σ modulator with *Q* enhanced *LC* tank circuits employing a single high *Q*-factor on-chip inductor and lesser quantizer levels thereby reducing the circuit complexity for excess loop delay, power dissipation and dynamic element matching. System level simulations indicate at a *Q*-factor of 75 Δ-Σ modulator with a 3-level quantizer achieves dynamic ranges of 106, 82 dB and 84 dB for RFID, TETRA, and Galileo over bandwidths of 200 kHz, 10 MHz and 40 MHz respectively.**



***Keywords-Q-enhancement, RF delta-sigma, on-chip inductor.***


## I. INTRODUCTION

Basic building blocks of continuous-time (CT) bandpass delta-sigma (Δ-Σ) modulators are CT second-order biquad filters, which can be implemented as transconductance-capacitor ($G_m$-$C$) filters or as inductor-capacitor ($LC$) tank circuits with former having limitations to high frequency signals [1]-[3]. Monolithic bandpass filters with on-chip $LC$ tuned circuits are therefore preferred from 100 MHz to over 1 GHz. The on-chip $Q$-factor $Q_o$ of the inductors is typically < 10, limited due to the operating frequency of the filter and the CMOS process. Various techniques are used to increase the $Q$-factor values to as much as to 20-170 [4]-[5]. For reconfigurable radio-frequency (RF) Δ-Σ modulator analog-to digital converters (ADC) the techniques employed become more challenging in view of multiple operating frequencies. Adequate dynamic range (DR) therefore is a challenge, which is overcome by employing multi-bit quantizers. However at RF sampling, as the quantizer levels increase so does the circuit complexity due to excessive loop delay (ELD), high power dissipation in the loop and dynamic element matching (DEM), restricting multi-bit quantizers to about 4 bits [6]. This paper gives an alternate approach that is able to employ a single optimised on-chip inductor for reconfigurability and high $Q$-factor, while minimizing the inductor layout, with which the Δ-Σ modulator is able to obtain adequate DR with a comparatively lower 3/5-level quantizer. The frequencies considered are for Radio Frequency Identification (RFID), Terrestrial Trunked Radio (TETRA) and the European Global Positioning System (GPS) Galileo. RFID integration with cellular/mobile technology such as GSM/LTE and GPS overcomes the short-range limitations in commercial and public safety applications [7]-[10]. As secure data is an important criterion TETRA is considered as the cellular standard in this paper [11]. RFID has a channel bandwidth of 200 kHz [12]. A channel bandwidth of 10 MHz is considered for TETRA considering the broadband requirements for Public Mobile Radio (PMR) [13]. For Galileo the E6A Public Regulated Signal (PRS) band for PMR is considered with a channel bandwidth of 40 MHz [14]. The DR requirements of the Δ-Σ ADC are analysed in section II. Section III details the on-chip inductor optimization, followed by simulations results in section IV. Conclusions are given in section V.

## II. DYNAMIC RANGE REQUIREMENTS Δ-Σ ADC

A receiver with signal levels is shown in Fig.1 where $R_s$ is the reference signal sensitivity. The RF filter is followed by a low noise amplifier (LNA) and a voltage gain amplifier (VGA) with an automatic gain control (AGC).

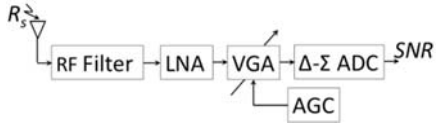


Fig. 1. Receiver front-end signal level.

The values of $R_s$ and downlink frequencies $f_o$ for RFID, TETRA and Galileo are summarised in TABLE 1.

| Standard | Channel | $R_s$ (dBm) | $f_o$ (MHz) |
|---|---|---|---|
| **RFID[12]** | 100 mW | -83 | 865.6 |
| | 101-500 mW | -90 | |
| | 501 mW-2 W | -96 | |
| **TETRA[11]** | π/4-, π/8-DQPSK | -112, -107 | 392 |
| | 4-QAM 25 kHz | -113 | |
| | 64-QAM 150 kHz | -105 | |
| **Galileo[14]** | E6A PRS | -125 | 1278.75 |

TABLE 1. Receiver front-end specifications

If the maximum power of a signal at the Δ-Σ ADC input is $P_{max}$ then the DR requirement for the Δ-Σ ADC is given by:

$$DR = P_{\max} - (R_s - 10dB) \quad (1)$$

This is considering a 10 dB margin below $R_s$ for the required SNR. A 15 dB gain is assumed for the LNA. The VGA with the AGC is able to keep $P_{max}$ to a an intermediate value of about -45 dBm despite the combined effects of RF filtering, fading and peak-to average power ratio (PAPR) as the VGA/AGC can offer typically a variable gain of ± 20 dB. In case the signal power is greater than interference, from (1) and TABLE 1 the DR

requirements are 61, 78 dB and 90 dB for RFID, TETRA and Galileo respectively. In case signal power is less than interference the minimum detectable signal must be 3 dB above $R_s$ [11], [12], [14]. The interference levels in case of TETRA and RFID are given in Fig. 2 [11], [15], [16], [17]. Since Galileo supports only one channel of reception, there are no interference specifications in the standards. However as the receiver must be immune to interference from other systems, a blocking level of -30 dBm is assumed from 0-1000 MHz and 1600-5000 MHz.

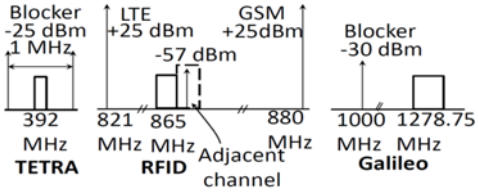


Fig. 2. Receiver interference levels.

Assuming the current available RF filter specifications, in Fig 3 $S_P$ are the interference (top row) and signal $R_s$ + 3dB (2nd row) levels in the receiver stages, δ the filter attenuation /insertion loss (-3 dB) and $L_G$ is the LNA gain of +15 dB. Due to the minimum detectable signal level the VGA offers a full gain of +20dB. The DR at the Δ-Σ modulator input is obtained by the difference in $S_P$ levels for interference and the signal. With the values obtained for DR in Fig.3 and allowing a further 10 dB margin the DR increase to 66 dB, 73 dB and 50 dB for RFID, TETRA and Galileo respectively. For final DR the maximum the two cases i.e. signal less and greater than interference are taken as 66, 78 dB and 90 dB for RFID, TETRA and Galileo respectively.

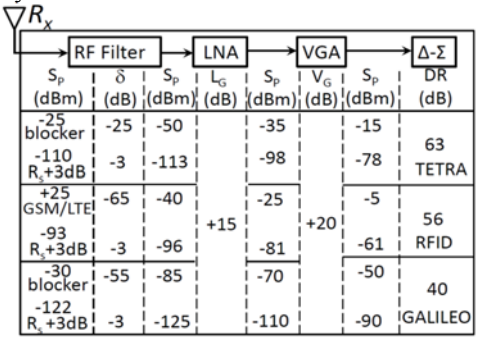


Fig. 3. Receiver signal and interference levels.

## III. ON-CHIP INDUCTOR OPTIMIZATION

Due to the mixed signal nature of the CT Δ-Σ modulator the loop filter coefficients must match their discrete-time (DT) equivalent, which is done using the impulse-invariant transform (IIT) [18]. To ensure sufficient degrees of freedom to match the loop coefficients finite-impulse response (FIR) digital-to-analog converter (DAC) in the feedback path are employed [19]. The 6th-order CT Δ-Σ modulator is shown in Fig 4 consisting of three *LC* tanks each having a 2nd-order biquad loop transfer function $H(s)$. There are three transconductance stages $G_{m1}$, $G_{m2}$ and $G_{m3}$ that transfer the input voltage to current which is then injected into the *LC* tank. A non-return-to-zero (NRZ) DAC pulse is used in the feedback path as it offers higher immunity to clock jitter than a return-to-zero (RZ) or a halfway-return-to-zero (HRZ) DAC pulse.

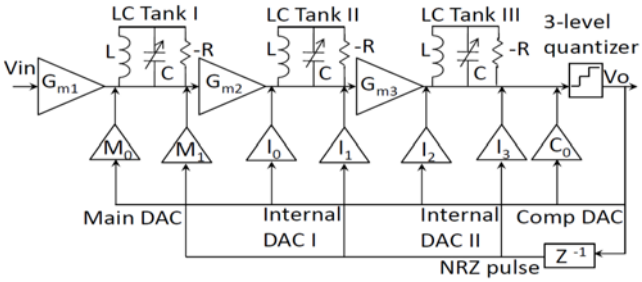


Fig. 4. Architecture of 6th-order CT BP Δ-Σ ADC.

In Fig. 5a $R_s$ is the inductor loss that is compensated by the parallel resistor $-R$ to cancel the loss equivalent to $R_s$ represented by $R_P$. The tank circuit is shown in Fig 5b wherein a cross-coupled transistor pair $M_{Qe1}$, $M_{Qe2}$ with transconductance $G_{mQ}$ is used such that negative resistance $-R$ can be adjusted by changing the bias source $I_{QE}$. Transistors $M_1$, $M_2$ are the input buffer stage and $M_3$, $M_4$ are varactors used to tune to the centre frequency $f_o$. The enhanced $Q$-factor $Q$ of the inductor is given by:

$$Q = \frac{Q_0}{1 - G_{mQ} R_P} \tag{2}$$

The transistor pair $M_{Qe1}$, $M_{Qe2}$ and range of $G_{mQ}$ may not be optimal for inductor loss compensation since the inductor parameters $R_s$ and $L$ depend on the process and $f_o$. The parameters need to be quantified to achieve the best $Q$-factor possible for all the operating $f_o$ with a single inductor. Employing multiple inductors in a single tank circuit is not a feasible option. An inductor with a high $Q_o$ is not necessarily the best choice as it may not offer adequate $Q$-factor for all $f_o$ with $Q$-enhancement. An inductor $L$ that matches the required $H(s)$ of the Δ-Σ modulator need not be optimal, as similar inductances have different $R_s$ and number of turns, which requires minimisation for reducing losses and the layout. The inductor choice is based on minimal layout and or on the transfer function only, which may not be optimal [18]-[22]. To the best knowledge of the authors there is a gap in the current approaches that can meet these requirements coherently for a reconfigurable RF Δ-Σ modulator design.

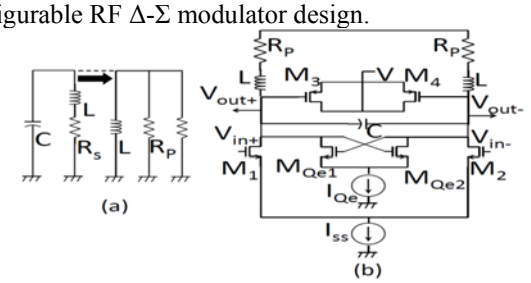


Fig. 5. $Q$-enhanced $LC$ tank circuit.

An octagon spiral CMOS inductor is shown in Fig. 6 specified by the number of turns $N$, the turn spiral width $W_S$, the under-pass width $W$, the turn spacing $S$, and any of the diameters inner $d_{in}$ or outer $d_{out}$. Depending on the geometrical specifications the inductor circuit parameters $L$, $R_s$ and $Q_o$ can be extracted using π, 2π lumped model and simulation tools such as SPECTRE RF

Cadence® or SONNET®. For various values of $N$, $W_S = W$, $S$ and $d_{in}$ the circuit parameters for 20 inductors were extracted in the frequency range of 0-2 GHz using SONNET ® for a 0.18 µm CMOS process. Layout values for five inductors with least $N$ and maximum $Q_o$ are given in TABLE 2.

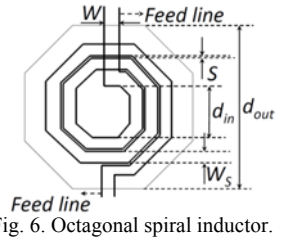

Fig. 6. Octagonal spiral inductor.

| Inductor | $W_s$ (µm) | $d_{in}$ | N | S (µm) |
|---|---|---|---|---|
| $L_1$ | 8 | 200 | 2.5 | 2 |
| $L_2$ | 8 | 200 | 4.5 | 2 |
| $L_3$ | 10 | 320 | 6.5 | 2 |
| $L_4$ | 10 | 280 | 3.5 | 3 |
| $L_5$ | 10 | 360 | 6.5 | 2 |

TABLE 2. Spiral inductor parameters

The extracted values of $Q_o$, $L$ and $R_s$ for the five inductors are plotted in Figs 7-9 respectively.

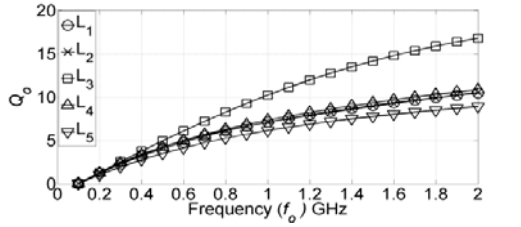

Fig. 7. Variation of $Q_o$ with $f_o$.

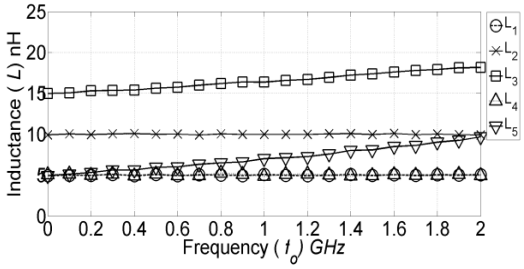

Fig. 8. Variation of $L$ with $f_o$.

Although $L_3$ has the maximum $Q_o$ it also has the highest $R_s$ and $N$, which may not be optimal in terms of minimising the losses and layout. Further analysis are also required to ensure that the inductor has sufficient $Q$ at all the $f_o$ frequencies employing the $Q$ enhancement in section *B*.

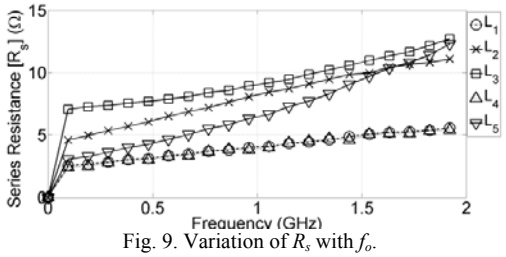

Fig. 9. Variation of $R_s$ with $f_o$.

The enhanced $Q$ values obtained reach a maximum followed by a discontinuity and high negative values, before settling down to moderate positive values for the remainder variation in $f_o$ and $G_{mQ}$. The values $f_o$ and $G_{mQ}$ for which $Q \geq 75$ are plotted in Fig 10. Only $L_1$ and $L_4$ offer $Q \geq 75$ for RFID, TETRA and Galileo, both have similar extracted parameters including $R_s$, however $L_1$ is the preferred choice as it has the least $N$.

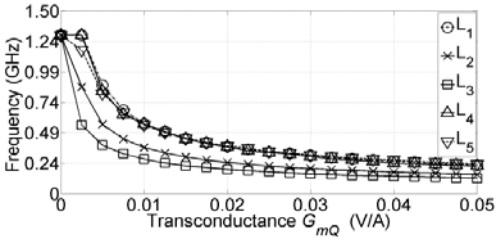

Fig. 10 Frequency ($f_o$), transconductance ($G_{mQ}$) for $Q \geq 75$.

The design methodology adopted in given in Fig. 11, which can be used to design the reconfigurable CT Δ-Σ modulator for multiple frequencies $f_1$, $f_2$, $f_3$,..$f_n$. The parameter extraction is undertaken for various frequencies and the optimal inductance value employed in the transfer function. DAC coefficients are obtained via the IIT with the optimised inductance value. For various $Q$-factor values the Δ-Σ modulator system level simulations are undertaken and the DR quantified against the minimum $DR_{min}$ for each of the frequencies from the standard specifications and the RF front-end (FE).

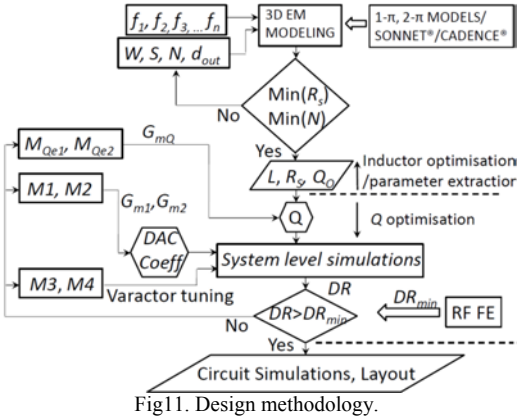

Fig11. Design methodology.

With the design methodology in Fig. 11 $G_{m1}$ is 90mA/V while $G_{m2}$ and $G_{m3}$ are 4mA/V, the FIR DAC coefficients obtained are implemented as current steering DACs in view of the high sampling rates required with bipolar current sources as signed digit code. As the sampling frequency $f_s$ is $4f_o$, the final sampling frequencies taken are as 1.712 GHz, 3.424 GHz (2×1.712 GHz) and 5.1136 GHz (3×1.712 GHz) simplifying the requirements for hardware implementation. The bandwidths are as per section I.

## IV. Simulation Results

Simulations are taken for the design parameters in section III in Matlab/Simulink R2013b for a time of period of 1ms. Output spectra for RFID, TETRA and Galileo in Fig. 12 indicate a smooth bandpass NTF response at the respective frequencies.

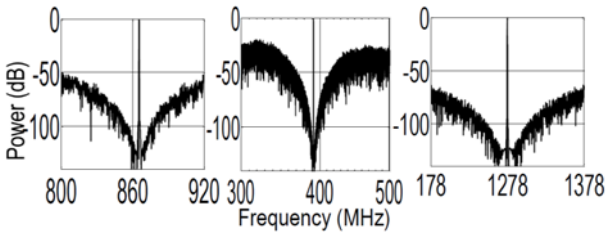


Fig.12. Output signal spectra for RFID, TETRA and Galileo.

Variations in DRs for a 3- and 5-level quantizer at different values of *Q*-factor are shown in Fig. 13. At $Q = 75$, for a 3-level quantizer the DR is 106, 82 and 84 dB, increasing to 110, 100 and 105 dB for the 5-level quantizer, for RFID, TETRA and Galileo respectively.

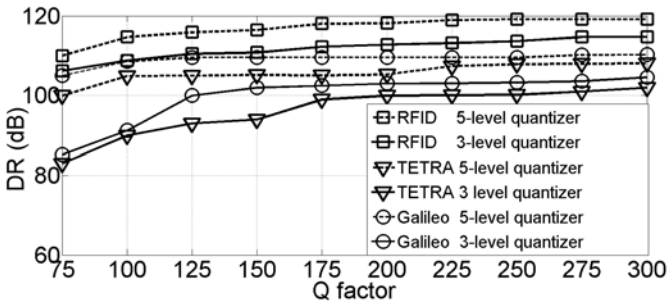


Fig.13. Δ-Σ modulator DR variation with Q factor.

A comparison of the existing reconfigurable Δ-Σ modulator designs in with this work is given in TABLE 3, where *O* is the Δ-Σ modulator order, *R* indicates if a single on-chip inductor is employed for reconfigurability and *M* the quantizer levels with power consumption. Within brackets indicated is the frequency/bandwidth in MHz.

| | *O* | DR (dB) | | | *R* | *M* |
|---|---|---|---|---|---|---|
| | | RFID | TETRA | Galileo | | |
| This work | 6 | 106, 110 (865.6/0.2) | 82, 100 (392/10) | 84, 105 (1278.75/40) | Y | 3, 5 |
| [20] | 4 | 52-42 (796.5/1) | - | 42 (1000/1) | Y | 3 (41 mW) |
| [21] | 6 | 77 (800/35) | 85 (400/35) | 75 (1000/35) | N | 17 (550 mW) |
| [22] | 4 | - | - | 48 (4500-5800/500) | Y | 2 (2.09 W) |
| [23] | 4 | - | - | 50-93 (1000-4000/NA) | N | 16 (NA) |

TABLE 3. Comparison with existing reconfigurable Δ-Σ modulators.

## V. CONCLUSIONS

As the on-chip inductor parameters depend on the process and operating frequencies, *Q*-enhancement for the *LC* biquad filters may not be efficient for the required inductor loss compensation. In reconfigurable CT RF Δ-Σ modulators the complexity increases due to multiple RF frequencies. An inductor with a high stand alone *Q*-factor is not the best choice, as it may not achieve high enhanced *Q*-factor for all the RF frequencies. The inductor value that matches the transfer function may not be optimal for power dissipation and layout. An approach that can meet these requirements for designing RF Δ-Σ modulators is given and is applied to a multi-standard design for RFID, TETRA and Galileo. It employs a single optimised on-chip inductor for reconfigurability, high *Q*-factor and minimal layout. Alternatively multi-bit quantizers can be employed, but the complexity at RF increases due to ELD, high power dissipation and DEM. The comparable levels of DR obtained from the existing reconfigurable Δ-Σ modulator designs require 16- and 17-level quantizers as compared to the proposed design with a comparatively a lower 3/5-level quantizer as observed in TABLE 3. The CMOS implementation for the design are currently underway, the results of which would be published in a future publication.

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